

WHAT IS CLAIMED IS:

1. Memory controller driver circuitry, comprising:
 - a data pad;
 - N data propagation circuits ($N \geq 2$);
 - a multiplexing stage which provides data to at least N-1 of the N data propagation circuits, said multiplexing stage enabling a coupling of a first data input stream to each of the N data propagation circuits when the multiplexing stage is configured in a 1x mode, and said multiplexing stage enabling a coupling of different data input streams to various of the N data propagation circuits when the multiplexing stage is configured in an Mx mode ($1 < M \leq N$); and
 - output merging circuitry which alternately couples the N data propagation circuits to the data pad to thereby generate either a 1x or Mx stream of data bits at the data pad.
2. Memory controller driver circuitry as in claim 1, further comprising:
 - a strobe pad; and
 - means for producing at said strobe pad an Mx strobe signal which corresponds to said Mx data stream.
3. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises N sequentially clocked flip-flops which respectively receive and output data from the N data propagation circuits.
4. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises a multiplexer which receives and sequentially outputs data from the N data propagation circuits.
5. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises N tri-statable paths which respectively

receive and sequentially output data from the N data propagation circuits.

6. Memory controller driver circuitry as in claim 5, wherein each of said N tri-statable paths comprises one of N sequentially clocked flip-flops.
7. Memory controller driver circuitry as in claim 1, wherein $N=M=2$.
8. Memory controller driver circuitry as in claim 1, wherein a first of the N data propagation circuits is a simple wire route.
9. Memory controller driver circuitry as in claim 1, wherein said data pad is a bidirectional data pad.
10. A double data rate memory controller, comprising:
 - a plurality of data and strobe pads;
 - means for writing data and generating strobes via said pads at 1x double data rate memory speed; and
 - means for writing data and generating strobes via said pads at Mx double data rate memory speed ($M \geq 2$).
11. A method of driving data from a memory controller, comprising:
 - providing data pad driver circuitry of said memory controller with a first data stream when said memory controller is configured to operate in a 1x mode;
 - providing said data pad driver circuitry with N-1 additional data streams when said memory controller is configured to operate in an Nx mode ($N \geq 2$); and
 - clocking said data pad driver circuitry at an Nx rate to thereby:
 - i) generate a 1x data stream at a data pad of said memory controller when said memory controller is configured to operate in 1x mode; and

- ii) generate an Nx data stream at said data pad when said memory controller is configured to operate in Nx mode.

12. A method as in claim 11, further comprising:

providing strobe pad driver circuitry of said memory controller with a set of signals which toggle at a 1x rate when said memory controller is configured to operate in a 1x mode;

providing said strobe pad driver circuitry with a set of static signals when said memory controller is configured to operate in an Nx mode; and

clocking said strobe pad driver circuitry at an Nx rate to thereby:

- i) generate a 1x strobe signal at a strobe pad of said memory controller when said memory controller is configured to operate in 1x mode; and
- ii) generate an Nx strobe signal at said strobe pad when said memory controller is configured to operate in Nx mode.

13. A method as in claim 11, wherein $N=2$.

14. A method as in claim 13, wherein clocking said data pad driver circuitry at an Nx rate comprises clocking first and second flip-flops which are coupled to said data pad via their outputs, said first flip-flop being positive edge triggered, and said second flip-flop being negative edge triggered, wherein each of said first and second flip-flops receives an Nx clock signal.

15. A method as in claim 11, wherein said first data stream is a double data rate data stream, and said 1x data stream is a double data rate data stream.

16. A method as in claim 11, wherein each of said first and N-1 additional data streams is a double data rate data stream.

17. A computer system, comprising:

- a CPU;
- a memory controller coupled to said CPU;
- an I/O controller coupled to said CPU;
- a number of I/O devices coupled to said I/O controller; and
- a number of memory modules coupled to said memory controller;

wherein said memory controller comprises a plurality of data pads to which is coupled data driver circuitry for driving data to said memory modules; and

wherein said data driver circuitry comprises, for each data pad:

- i) N data propagation circuits ($N \geq 2$);
- ii) a multiplexing stage which provides data to at least N-1 of the N data propagation circuits, said multiplexing stage enabling a coupling of a first data input stream to each of the N data propagation circuits when the multiplexing stage is configured in a 1x mode, and said multiplexing stage enabling a coupling of different data input streams to various of the N data propagation circuits when the multiplexing stage is configured in an Mx mode ($1 < M \leq N$); and
- iii) output merging circuitry which alternately couples the N data propagation circuits to the data pad to thereby generate either a 1x or Mx stream of data bits at the data pad.

18. A computer system as in claim 17, wherein the memory controller further comprises a plurality of strobe pads to which is coupled strobe driver circuitry for driving strobes to said memory modules, said strobe

driver circuitry comprising means for producing Mx strobe signals at said strobe pads.

19. A computer system as in claim 17, wherein for each data pad, said output merging circuitry comprises N tri-statable paths which respectively receive and sequentially output data from the N data propagation circuits.
20. A computer system as in claim 17, wherein $N=M=2$.
21. A computer system as in claim 17, wherein said memory controller and said I/O controller form an integrated memory and I/O controller.